IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

ANTONIO E. SALLOUM SALAZAR | PHN 16,542A

Serial No.

Filed: CONCURRENTLY

Title: A PROCESSING DEVICE FOR EXECUTING VIRTUAL MACHINE INSTRUCTIONS THAT INCLUDES INSTRUCTIONS REFEEDING MEANS

Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-14 without prejudice.

Please add the following new claims:

15. (New) A processing device for executing virtual machine instructions; the processing device comprising:

an instruction memory for storing instructions including at least one of the virtual machine instructions;

a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions; the native instructions being different from the virtual machine instructions; and

a pre-processor comprising:

a converter for converting at least one virtual machine instruction, fetched from the instruction memory into at least one native instruction; and

feeding means for feeding native instructions to the microcontroller core for execution;

characterized in that

the processing device is a stack oriented machine, that at least the top elements of the stack are mapped onto registers of the microcontroller and in that the position of the top of the register stack is indicated using a register of the converter.

16. (New) A processing device according to claim 1, characterized in that the converter converts a virtual machine instruction into native instructions under control of micro code.

17. (17) A processing device according to claim 2, characterized in that said conversion includes the calculation of indications for argument registers for the native instructions from a value in the said register of the converter.

18. (New) A processing device according to claim 2 or 3, characterized in that the virtual machine instruction is the Java byte code 'bipush n', said code being converted into a sequence of native MIPS instructions.

19. (New) A processing device according to one of the previous claims, characterised in that:

the processor is of a type which after the occurrence of a predetermined condition, such as an interrupt, requests re-feeding of up to a predetermined maximum of n native

instructions, where n > 1; and

the feeding means comprises means for in response to the processor requesting re-feeding of a number of native instructions, re-feeding the requested native instructions.

20. (New) A processing device as claimed in claim 5, characterised in that the pre-processor comprises a feeding memory for storing at least n instructions which were last fed to the processor; and

in that the feeding means is operative to, in response to the processor requesting re-feeding of a number of instructions, re-feeding the requested instructions from the feeding memory.

21. (New) A pre-processor for use with a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions;

the pre-processor comprising:

a converter for converting at least one virtual machine instruction, fetched from an instruction memory, into at least one native instruction; the native instructions being different from the virtual machine instructions; and

feeding means for feeding native instructions to the microcontroller core for execution;

characterised in that the

pre-processor and the processor are part of a stack oriented machine, that at least the top elements of the stack are mapped onto registers of the microcontroller and in that the position of the top of the memory stack is indicated using a register of the converter.

22. (New) A pre-processor according to claim 7, characterized in that the converter converts a virtual machine instruction into native instructions under control of micro code.

23. (New) A pre-processor according to claim 8, characterized in that said conversion includes the calculation of indications for argument registers for the native instructions from a value in the said register of the converter.

24. (New) A processing device according to claim 8 or 9, characterized in that the virtual machine instruction is the Java byte code 'bipush n', said code being converted into a sequence of native MIPS instructions.

REMARKS

It is respectfully submitted that the patent application is now in proper form for allowance. Accordingly, allowance of the patent application is earnestly solicited.

However, should the Examiner believe that direct contact with the Applicants' attorney would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

Respectfully submitted,

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